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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHERY, DADY	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,915	BHANDARI ET AL.	
	Examiner	Art Unit	
	Dady Chery	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6,7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Fellman et al. (US Patent 6,246,702 hereinafter Fellman).

Regarding claim 1, Fellman discloses *a method for synchronizing clocks of network terminals in a network* (Fig. 2), *comprising:*

selecting a clock of one of said network terminals to be a master clock (Col. 14, lines 41 – 45);

determining a respective round trip delay time from said network terminal having said master clock to each of said other terminals (Col. 15, lines 40 –42) ;

offsetting the clock of each of said other terminals by an amount proportional to the respective determined round trip delay time such that said network terminal having said master clock and each of said other terminals have substantially the same point of reference in time (Col. 15, lines 55 - Col. 16, lines 8);

in response to at least one trigger signal (Cool. 7, lines 60 – 64), *determining a respective offset between the master clock and the clocks of each of said other terminals and offsetting the clocks of each of said other terminals by an amount proportional to said determined respective offset to synchronize the clocks of each of said other terminals to said master clock* (Col. 15, lines 36 – Col. 16, lines 7);

Regarding claim 2,Fellman discloses *the selected network terminal comprises a master terminal* (Col. 10, lines 64 –66).

Regarding claim 3, Fellman discloses *the other network terminals comprise slave terminals* (Col. 11, lines 6 –8).

Regarding claim 4, Fellman discloses the method wherein the determining a respective round trip delay time, comprises:

transmitting a respective data packet from said terminal including the master clock to each of said other terminals(Col. 15, lines 38 –39);

and determining, from respective data packets received from each of said other terminals in response to said transmitted respective data packets, a respective amount of time for data packets to be transmitted to and received from each of said other terminals (Col. 15, lines 39 –43).

Regarding claim 6, Fellman discloses *each of the other terminals respectively triggers the synchronization of its respective clock to the master clock* (Col. 7, lines 60m –65).

Regarding claim 7, Fellman discloses *a network for synchronizing clocks of network terminals in said network* (Fig. 2), comprising:

a synchronization device (100) *for providing a timing signal* (Col. 10, lines 64 – 65);

a master terminal (1000), including:

a master clock (Fig. 3,1010) *for providing timing information for said master terminal* (Col. 10, lines 29 –30);

a master network interface controller (1004) *for transmitting data from and receiving data for said master terminal* (Col. 10, lines 25 –26);

a master control unit (1000) *for determining synchronization parameters* (Col. 10, lines 16 – 19);

a plurality of slave terminals (1000), *each of said slave terminals including*:

a slave-clock (1010) *for providing timing information for said slave terminal* (Col. 11, lines 6 –8);

a slave controller for making adjustments to said slave-clock in response to a control signal indicative of a difference between said master clock and said slave-clock (Col. 11, lines 9 –11)

a slave network interface controller (1008) *transmitting data from and receiving data for said slave terminal* (Col. 10, lines 24 –26)

a non-blocking switch (2) *for interconnecting said master terminal and said plurality of slave terminals;*

wherein said master control unit comprises a memory (1012) *and a processor* (1002) *and is adapted to perform a method comprising* (Col. 10, lines 28 –30):

determining a respective round trip delay time for each of said plurality of slave terminals; communicating a control signal to respective slave controllers of the plurality of slave terminals for offsetting the slave-clock of each of said slave terminals by an amount proportional to the respective determined round trip delay time such that said master terminal and each of said slave terminals have substantially the same point of reference in time (Col. 11, lines 6 – 15 and Col. 15,lines 36 – 46);

determining a respective offset between the master clock and a respective slave-clock of each of said slave terminals in response to information received from each of said slave terminals regarding a status of the respective slave-clocks (Col. 15, lines 36 – Col. 16, lines 7);

offsetting a respective slave-clock of each of said slave terminals by an amount proportional to said determined respective offset to synchronize the slave-clock of each of said slave terminals to the master clock of said master terminal (Col. 15, lines 36 – Col. 16, lines 7)..

Regarding claim 10,Fellman discloses *the synchronization device generates a time frame for the synchronization of the respective slave-clocks of said plurality of slave terminals to the master clock of said master terminal* (Col. 15, lines 25 –33 and lines 65 – 68).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fellman as applied to claim1 above, and further in view of Lehr et al. (US Patent 4,005,266, hereinafter Lehr.

Regarding claim 5,Fellman discloses all the limitations of claim 5, except *the respective offset for each of the other terminals is determined comprising:*
in response to a synchronization signal, counting a predetermined number of clock pulses of said master clock;
counting clock pulses of the clocks of said other terminals for a period of time equal to the amount of time for counting said predetermined number of clock pulses of said master clock and beginning at a point in time of said synchronization signal; and
comparing the phase and frequency of the counted clock pulses of each of the other terminals to the clock pulses of said master terminal to determine a respective offset.

However, Lehr teaches *the respective offset for each of the other terminals is determined comprising:*

in response to a synchronization signal, counting a predetermined number of clock pulses of said master clock;

counting clock pulses of the clocks of said other terminals for a period of time equal to the amount of time for counting said predetermined number of clock pulses of said master clock and beginning at a point in time of said synchronization signal; and

comparing the phase and frequency of the counted clock pulses of each of the other terminals to the clock pulses of said master terminal to determine a respective offset (Col. 6, lines 60 –Col. 7, lines 19). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Lehr into the teaching of Fellman for the purpose of using a counter to count the number of internal clock signals period during a configurable a number of additional clocks for the purpose of determine the number of correction of a system cycles (Abstract).

Regarding claim 8, Fellman discloses each of said network interface controllers comprises:

Fellman discloses *a transmit trigger generator* (100) *for receiving the signal from said counter and, in response, generating a transmit trigger signal* (Col. 7, lines 54 –65); Where the resolution synchronization signal is considered as trigger signals

a transmit memory device (1012), for storing data to be transmitted (Col. 10, lines 28 – 34);

a transmit memory manager (1002) for receiving the transmit trigger signal from said transmit trigger generator and, in response, directing at least a portion of said data stored in said memory device to a transmission device for transmission of said data (Col. 10, lines 23 – 36); Where the processor is considered as the transit memory manager

a receive trigger generator (100) *for receiving the signal from said counter and, in response, generating a receive trigger signal* (Col. 7, lines 54 –56 and Col. 10, lines 24 – 36);

a receive memory device (1012), *for storing received data*(Col. 10, lines 28 – 34);

a receive memory manager for receiving the receive trigger signal from said receive trigger generator and, in response, directing received data to a location within said receive memory device (Col. 10, lines 23 – 36); Where the processor is considered as the receive memory manager.

Fellman fails to mention *the counting device for generating a signal in response to counting a predetermined number of counts*;

However, Lehr teaches a main counter and a secondary counter (Fig. 2, 30 and 35) that is considered as counting device for generating a signal in response to counting a predetermined number of counts (Col. 6, lines 61 – Col. 7, lines 20 and Col.10, lines 52 –Col. 11, lines 22). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a counter for generating a signal in response to counting a predetermined number of counts signals period during a configurable a number of additional clocks for the purpose of determine the number of correction of a system cycles (Abstract).

Regarding claim 9, Fellman discloses all the limitations of claim 9 as applied to claim 8 above except *each of said counting devices begins counting from a predetermined count number in response to a timing signal from said synchronization device.*

However, Lehr teaches *each of said counting devices begins counting from a predetermined count number in response to a timing signal from said synchronization device* (Col. 7, lines 1 –10 and Col. 10 , lines 54 – Col. 11, lines 6).

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made the counter begins counting from a predetermined number for the purpose of control the error value (Col. 11, lines 12 – 20).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fellman as applied to claim 7 above, and further in view of Lundh et al. (US Patent 6,373,834, hereinafter Lundh).

Regarding claim 11,Fellman discloses all the limitations of claim 11 as applied to claim 7, except *the master terminal transmits a data packet having a Sync header and a timing signal to each of said plurality of slave terminals to cause each of said slave*

terminals to transmit information regarding a status of their respective slave-clocks to the master terminal.

However, Lundh teaches *the master terminal transmits a data packet having a Sync header and a timing signal to each of said plurality of slave terminals to cause each of said slave terminals to transmit information regarding a status of their respective slave-clocks to the master terminal* (Col. 12, lines 2 – 25). Where the ANANLYZE_SFC is considered as the Sync header.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Lundh into the teaching of Fellman for the purpose of synchronizing a master timing unit and plurality of slave unit device (Abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dady Chery whose telephone number is 571-270-1207. The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dady Chery 08/01/2007

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER